

Scaffolded Electronics Design Studio: Reporting, Soldering, Simulation and Bilingual First Year Success in a China Joint Education Programme

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CONTEXT AND RATIONALE

First year engineering students on bilingual China Joint Education Programmes are required to master circuit theory, laboratory practice, academic writing and specialist software concurrently, often in a second language and without established study habits. This poster reports on a five phase scaffolded design studio, delivered within the Praxis Electronics Design module (B37VA) across two China based cohorts (Ocean University of China and Xidian University, n = 133), developed to reduce cognitive overload while preserving academic rigour and building disciplinary identity.

RESEARCH QUESTIONS

- RQ1: How do early academic literacy support, including report templates, exemplars and referencing workshops, influence report quality and feedback assimilation?
- RQ2: Does sequencing simulation, then soldering and PCB assembly, then an integrated mini project, enhance practical competence and troubleshooting confidence?
- RQ3: Which of these supports the most benefit bilingual students in terms of readiness, engagement, sense of belonging and performance on communication-oriented assessment criteria?

METHODOLOGY

The evaluation follows a mixed-methods, enhancement-oriented single delivery cycle, with the prior cohort used as an informal comparator. Four data strands were combined: quantitative rubric ratings of report structure and argumentation together with learning analytics; a pre- and post-self-efficacy survey addressing writing, simulation and soldering competence; qualitative focus groups and reflective prompts, with deliberate oversampling of bilingual students; and teaching team moderation notes documenting rubric clarity and feedback consistency across delivery.

KEY FINDINGS

- Templates and exemplars were consistently praised, with students directly attributing report writing confidence to structured scaffolds and iterative feedback cycles.
- Sequencing simulation before physical soldering reduced error propagation, with students who debugged circuits virtually making fewer assembly mistakes on real PCBs.
- Checklist artefacts, covering PCB assembly and risk assessment, were cited as key enablers of independent working, reducing reliance on staff during laboratory sessions.
- Teacher patience and a deliberately slowed pace of delivery were flagged by students as critical to comprehension for those studying in a second language.
- Across both institutions, 100 per cent of respondents rated overall satisfaction as at least Satisfied (67 per cent Very Satisfied at Ocean University of China, n = 60; 51 per cent Very Satisfied at Xidian University, n = 73).

CONTRIBUTION AND IMPLICATIONS

The study offers a transferable and reproducible model for first-year practical engineering education, integrating academic literacies, safety artefacts, simulation sequencing and structured bilingual access, without any lowering of assessment standards. Consistent satisfaction across two distinct institutional contexts suggests the approach is robust to variation in cohort background. Planned future work includes longitudinal tracking of report quality, calibration of rubric application across teaching teams, and dedicated focus group analysis with bilingual students.